Intel Core (microarchitecture)

The **Intel Core microarchitecture** (previously known as the **Next-Generation Micro-Architecture**) is a multi-core processor microarchitecture unveiled by Intel in Q1 2006. It is based on the Yonah processor design and can be considered an iteration of the P6 microarchitecture, introduced in 1995 with Pentium Pro. The high power consumption and heat intensity, the resulting inability to effectively increase clock speed, and other shortcomings such as the inefficient pipeline were the primary reasons for which Intel abandoned the NetBurst microarchitecture and switched to completely different architectural design, delivering high efficiency through a small pipeline rather than high clock speeds. It is worth noting that the Core microarchitecture never reached the clock speeds of the Netburst microarchitecture, even after moving to the 45nm lithography.

The first processors that used this architecture were code-named **Merom**, **Conroe**, and**Woodcrest**; Merom is for mobile computing, Conroe is for desktop systems, and Woodcrest is for servers and workstations. While architecturally identical, the three processor lines differ in the socket used, bus speed, and power consumption. Mainstream Core-based processors are branded *Pentium Dual-Core* or *Pentium* and low end branded *Celeron*; server and workstation Core-based processors are branded *Xeon*, while desktop and mobile Core-based processors are branded as *Core 2*. Despite their names, processors sold as Core Solo/Core Duo and Corei3/i5/i7 do not actually use the Core microarchitecture and are based on the Enhanced Pentium M and newer Nehalem/Sandy Bridge microarchitectures, respectively.

Features

The Core microarchitecture returned to lower clock rates and improved the usage of both available clock cycles and power when compared with the preceding NetBurst microarchitecture of the Pentium 4/D-branded CPUs.[1] The Core microarchitecture provides more efficient decoding stages, execution units, caches, and buses, reducing the power consumption of Core 2-branded CPUs while increasing their processing capacity. Intel's CPUs have varied widely in power consumption according to clock rate, architecture, and semiconductor process, shown in the CPU power dissipation tables.

Like the last NetBurst CPUs, Core based processors feature multiple cores and hardware virtualization support (marketed as Intel VT-x), as well as Intel 64 and SSSE3. However, Core-based processors do not have the Hyper-Threading Technology found in Pentium 4 processors. This is because the Core microarchitecture is a descendant of the P6 microarchitecture used by Pentium Pro, Pentium II, Pentium III, and Pentium M.

The L1 cache size was enlarged in the Core microarchitecture, from 32KB on Pentium II/III (16 KB L1 Data + 16 KB L1 Instruction) to 64 KB L1 cache/core (32 KB L1 Data + 32 KB L1 Instruction) on Pentium M and Core/Core 2. It also lacks an L3 Cache found in the Gallatin core of the Pentium 4 Extreme Edition, although an L3 Cache is present in high-end versions of Core-based Xeons. Both an L3 cache and Hyper-threading were reintroduced in the Nehalem microarchitecture.

Technology

While the Core microarchitecture is a major architectural revision it is based in part on the Pentium M processor family designed by Intel Israel.[2] The Penryn pipeline is 12–14 stages long[3] — less than half of Prescott's, a signature feature of wide order execution cores. Penryn's successor, Nehalem has 16 pipeline stages.[3] Core's execution unit is 4 issues wide, compared to the 3-issue cores of P6,Pentium M, and 2-issue cores of NetBurst microarchitectures. The new architecture is a dual core design with linked L1 cache and sharedL2 cache engineered for maximum performance per watt and improved scalability.

One new technology included in the design is Macro-Ops Fusion, which combines two x86 instructions into a single micro-operation. For example, a common code sequence like a compare followed by a conditional jump would become a single micro-op.

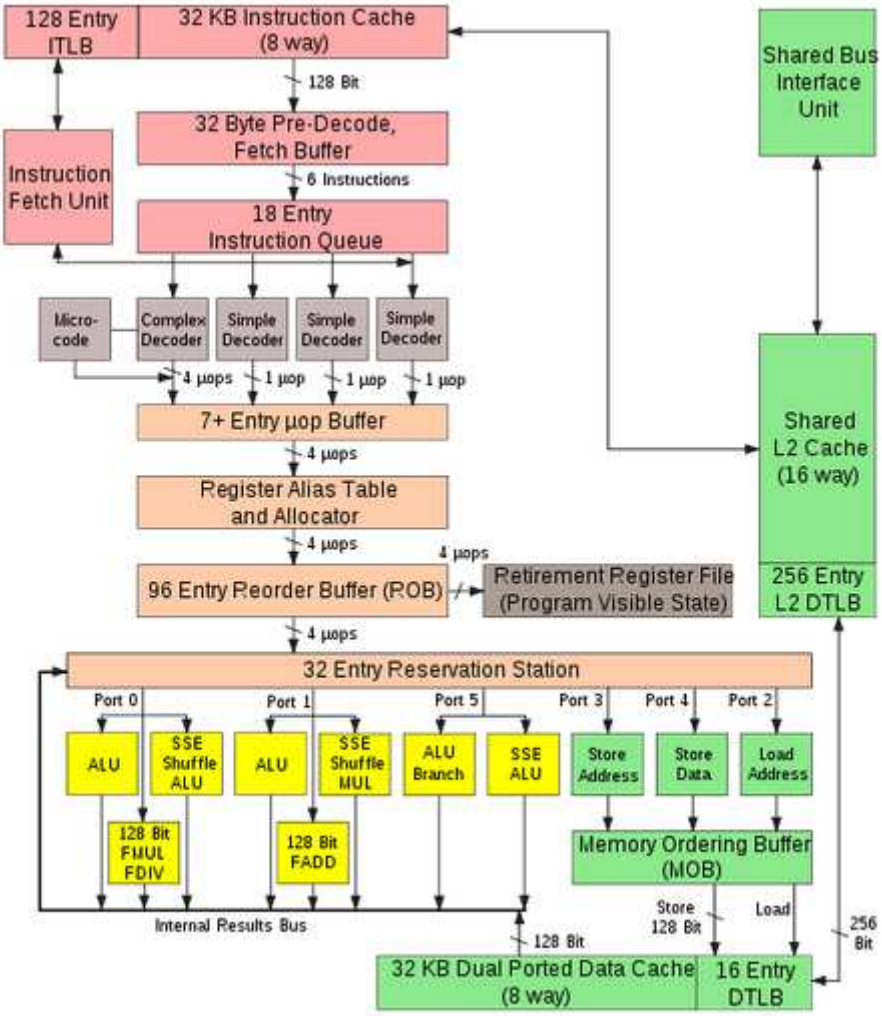
Other new technologies include 1 cycle throughput (2 cycles previously) of all 128-bit SSE instructions and a new power saving design. All components will run at minimum speed, ramping up speed dynamically as needed (similar to AMD's Cool'n'Quiet power-saving technology, as well as Intel's own SpeedStep technology from earlier mobile processors). This allows the chip to produce less heat, and consume as little power as possible.

For most Woodcrest CPUs, the front side bus (FSB) runs at 1333 MT/s; however, this is scaled down to 1066 MT/s for lower end 1.60 and 1.86 GHz variants.[4][5] The Merom mobile variant was initially targeted to run at a FSB of 667 MT/s while the second wave of Meroms, supporting 800 MT/s FSB, were released as part of the Santa Rosa platform with a different socket in May 2007. The desktop-oriented Conroe began with models having an FSB of 800 MT/s or 1066 MT/s with a 1333 MT/s line officially launched on July 22, 2007.

The power consumption of these new processors is extremely low—average use energy consumption is to be in the 1–2 watt range in ultra low voltage variants, with thermal design powers(TDPs) of 65 watts for Conroe and most Woodcrests, 80 watts for the 3.0 GHz Woodcrest, and 40 watts for the low-voltage Woodcrest. In comparison, an AMD Opteron 875HE processor consumes 55 watts, while the energy efficient Socket AM2 line fits in the 35 watt thermal envelope (specified a different way so not directly comparable). Merom, the mobile variant, is listed at 35 watts TDP for standard versions and 5 watts TDP for Ultra Low Voltage (ULV) versions.[*citation needed*]

Previously, Intel announced that it would now focus on power efficiency, rather than raw performance. However, at IDF in the spring of 2006, Intel advertised both. Some of the promised numbers were:

- 20% more performance for Merom at the same power level (compared to Core Duo)
- 40% more performance for Conroe at 40% less power (compared to Pentium D)
- 80% more performance for Woodcrest at 35% less power (compared to the original dual-core Xeon)



Intel Core 2 Architecture